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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,714	12/31/2003	Ricardo E. Gonzalez	PA2683US	1388

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EXAMINER	
GEIB, BENJAMIN P	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 04/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,714	GONZALEZ ET AL.	
	Examiner	Art Unit	
	Benjamin P. Geib	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *27-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Fritz Fleming
FRITZ FLEMING
Supervisory PRIMARY EXAMINER 4/14/2006
GROUP 2100
AU 2181

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/28/05, 02/21/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 have been examined.

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Application 12/31/2003, Declaration on 08/09/2004, Information Disclosure Statement on 04/28/2005, and Information Disclosure Statement on 02/21/2006.

Election/Restrictions

1. Claims 1-30 are presented for examination.

2. Restrictions to one of the following inventions is required under 35 USC § 121:

   a. Claims 1-26, drawn to a processing system containing multiple software extensible processing nodes that communicate with each other. Classified in Class 712, subclass 11.

   b. Claims 27-30, drawn to a method of routing a packet among a plurality of processing nodes. Classified in Class 709, subclass 238.

3. The inventions are distinct, each from the other because of the following reasons: Inventions a and b are related as sub-combinations disclosed as usable together in a single combination. The sub-combinations are distinct from each other if they are shown to be separately usable.

   In the instant case, invention a has separate utility such as a system or method for a processing system containing multiple software extensible processing

nodes that communicate with each other using routing method different than that disclosed for invention b (e.g. broadcast).

Invention b has separate utility such as for a method of routing a packet among a plurality of processing nodes that do not comprise or use the specific components disclosed for invention a.

4. Because these inventions are distinct for the reasons given above and would require divergent searches and have acquired a separate status in the art as shown by their different classification thus putting a serious burden on the examiner, restriction for examination purposes as indicated is proper.

5. During a telephone conversation with Eugene Kim on 04/05/2006 a provisional election was made with traverse to prosecute the invention of group a, claims 1-26. Affirmation of this election must be made by applicant in replying to this Office action. Claim 27-30 withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 4-9, 12, 14-15, 17-21, and 24-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Willis et al., U.S. Patent No. 5,999,734 (Herein referred to as Willis).

5. Referring to claim 1, Willis has taught a system for processing applications, the system comprising:

a plurality of processor nodes *[Fig. 1, components 11 & 12]* with each processor node comprising:

a processing element *[processor; Fig. 1, component 1]* configured to execute at least one of the applications *[column 6, lines 36-43]*;

a software extensible device *[re-configurable logic block; Fig. 1, component 9]* configured to provide additional instructions to a set of standard instructions for the processing element *[column 6, lines 1-8]*; and

a communication interface *[message interface; Fig. 1, component 10]* configured to communicate with other processor nodes *[column 5, lines 4-8]*; and

a plurality of links interconnecting the processor nodes *[links connecting the message interfaces (Fig. 1, components 10) to the message interconnect (Fig. 1, component 13)]*.

6. Referring to claim 4, Willis has taught the system of claim 1 wherein the plurality of the processor nodes are configured in an array *[The processing nodes are configured in an array with 2 columns and 1 row; See Fig.1]*.

7. Referring to claim 5, Willis has taught the system of claim 1wherein the software extensible device comprises an instruction set extension fabric *[The software extensible*

device (i.e. re-configurable logic block) comprises a fabric of re-configurable logic devices (See Fig. 2) that extend the instruction set; column 6, lines 1-8].

8. Referring to claim 6, Willis has taught the system of claim 1 wherein the software extensible device comprises a programmable logic device *[The software extensible device (i.e. re-configurable logic block) is a logic device that is programmable; column 5, lines 31-53].*

9. Referring to claim 7, Willis has taught the system of claim 1 wherein the communication interface *[message interface]* is configured to communicate using shared memory *[The message interface communicates with the processors within a processing node (Fig. 1, components 1 & 2) via shared memory; See Fig. 1, column 5, lines 20-30].*

10. Referring to claim 8, Willis has taught the system of claim 1 wherein the communication interface *[message interface]* is configured to communicate using message passing *[column 5, lines 4-8].*

11. Referring to claim 9, Willis has taught the system of claim 1 wherein the communication interface *[message interface]* is configured to communicate using channels between the processor nodes *[Since the processor nodes communicate with each other there are inherently channels of communication between the processor nodes; See Fig. 1; column 5, lines 4-8].*

12. Referring to claim 12, Willis has taught the system of claim 1 wherein the communication interface *[message interface]* comprises a processor network interface *[The message interface interfaces a network of processors; See Fig. 1].*

13. Referring to claim 14, Willis has taught the system of claim 1 wherein the communication interface comprises a standard input/output interface *[The message interface implements the IEEE standard 1596 protocol and, therefore, comprises a standard input/output interface; column 5, lines 4-9. Furthermore, any processor communication interface that implements input/output is inherently a standard input/output interface since it is the standard input/output interface for the system].*

14. Referring to claim 15, Willis has taught the system of claim 1 wherein the communication interface comprises an interface module configured to communicate between processor nodes on different chips *[The message interface is configured to communicate between processor nodes on different chips since whether or not the processor nodes are on different chips does not affect the communication interface; See Fig. 1; column 5, lines 4-8].*

15. Referring to claim 17, Willis has taught the system of claim 1 wherein at least one of the processor nodes is different from the other processor nodes *[The two processing nodes are two distinct devices and are, therefore, different; See Fig. 1].*

16. Referring to claim 18, Willis has taught a method for a system with multiple processor nodes, the method comprising:

executing an application in at least one processing element *[processor; Fig. 1, component 1]* in a plurality of the processor nodes *[Fig. 1, components 11 & 12; column 6, lines 36-43]*;

providing an additional instruction to a set of standard instructions for the processing element using at least one software extensible device *[re-configurable logic.*

block; Fig. 1, component 9] in the plurality of the processor nodes *[column 6, lines 1-8]*; and

communicating between the processor nodes using at least one communication interface *[message interface; Fig. 1, component 10]* in a plurality of the processor nodes *[column 5, lines 4-8]*.

17. Referring to claim 19, given the similarities between claim 7 and claim 19 the arguments as stated for the rejection of claim 7 also apply to claim 19.

18. Referring to claim 20, given the similarities between claim 8 and claim 20 the arguments as stated for the rejection of claim 8 also apply to claim 20.

19. Referring to claim 21, given the similarities between claim 9 and claim 21 the arguments as stated for the rejection of claim 9 also apply to claim 21.

20. Referring to claim 24, has taught the method of claim 18 further comprising compiling the application *[column 6, lines 36-43]*.

21. Referring to claim 25, Willis has taught the method of claim 18 further comprising loading the application into one of the plurality of the processor nodes *[It is inherent that in order for an application to be executed in a processor node the application is loaded into the node]*.

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. Claims 2, 3, 10, 11, 13, 16, 22, 23, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Willis.

24. Referring to claim 2,

Willis has taught the system of claim 1.

Willis has not explicitly taught that each one of the processor nodes is on a separate chip.

However, Examiner takes Official Notice that having each processor node on a separate chip is conventional and well-known.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Willis to have each processor node on a separate chip since doing so would reduce system cost.

25. Referring to claim 3,

Willis has taught the system of claim 1.

Willis has not explicitly taught that at least some of the processor nodes are on the same chip.

However, Examiner takes Official Notice that having some processor nodes on the same chip is conventional and well-known.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Willis to have some of the processor nodes on the same chip since doing so would reduce the total space consumed by the system.

26. Referring to claim 10,

Willis has taught the system of claim 9.

Willis has not explicitly taught that the communication interface is configured to perform time division multiplexing using the channels between the processor nodes.

However, Examiner takes Official Notice that communication interfaces configured to perform time division multiplexing using the channels between the processor nodes are conventional and well-known.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Willis so that the communication interface is configured to perform time division multiplexing using the channels between the processor nodes since doing so allows a single transmission path to be shared by multiple signals.

27. Referring to claim 11,

Willis has taught the system of claim 9.

Willis has not explicitly taught that the communication interface is configured to perform spatial division multiplexing using the channels between the processor nodes.

However, Examiner takes Official Notice that communication interfaces configured to perform spatial division multiplexing using the channels between the processor nodes are conventional and well-known.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Willis so that the communication interface is configured to perform spatial division multiplexing using the channels between the processor nodes since doing so increases data transmission speed.

28. Referring to claim 13,

Willis has taught the system of claim 1.

Willis has not explicitly taught that the communication interface comprises a processor network switch.

However, Examiner takes Official Notice that communication interfaces comprising a processor network switch are conventional and well-known.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Willis so that the communication interface comprises a processor network switch since doing so advantageously allows the connection of multiple network segments.

29. Referring to claim 16,

Willis has taught the system of claim 1.

Willis has not explicitly taught that the communication interface comprises a multiplexer/demultiplexer.

However, Examiner takes Official Notice that communication interfaces comprising a multiplexer/demultiplexer are conventional and well-known.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Willis so that the communication interface comprises a multiplexer/demultiplexer since doing so allows the combination of multiple data streams into a single data stream that can be advantageously transmitted over a single transmission link.

30. Referring to claim 22, given the similarities between claim 10 and claim 22 the arguments as stated for the rejection of claim 10 also apply to claim 22.

31. Referring to claim 23, given the similarities between claim 11 and claim 23 the arguments as stated for the rejection of claim 11 also apply to claim 23.

32. Referring to claim 26,

Willis has taught the method of claim 18.

Willis has not explicitly taught configuring one of the processor nodes to select between an interface module and a standard input/output interface based on a neighboring device.

However, Examiner takes Official Notice that configuring processor nodes to select between an interface module and a standard input/output interface based on a neighboring device is conventional and well-known.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Willis so that a processor node is configured to select between an interface module and a standard input/output interface based on a neighboring device since doing so would allow communication between the neighboring device and the processor node.

Conclusion

33. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or

patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin P. Geib whose telephone number is (571) 272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Benjamin P Geib
Examiner
Art Unit 2181

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4/14/2006